## REMARKS

The Office Action dated April 21, 2005 in this Application has been carefully considered. Claims 1-20 are pending. The above amendments and the following remarks are presented in a sincere attempt to place this Application in condition for allowance. Claim 10 has been amended in this Response. Claims 19 and 20 are new and are added in this Response. Reconsideration and allowance are respectfully requested in light of the above amendments and following remarks.

Applicants wish to thank the Examiner for the courtesy of the interview conducted on June 28, 2005. During the interview, the above-referenced amendments were discussed. However, tentative agreement was not reached that such amendments patentably distinguish from the art currently of record.

Claims 1-18 stand rejected under 35 U.S.C. §103(a) by U.S. Patent No. 5,555,382 by Thaller et al. ("Thaller") in view of U.S. Patent No. 6,754,838 B2 by Burns et al. ("Burns"). Insofar as they may be applied against the Claims, these rejections are overcome/traversed.

Regarding Claim 1, Thaller was cited as assertedly fully disclosing the following:

(1) "a first microprocessor having one or more interfacing logics including a first interfacing logic, the first microprocessor being clocked by a first system clock (*fig. 2, items 14, 202, 226, 234-236, 260; column 7, lines 27-53*)" (Office Action at 2);

(2) "a memory controller connected to the first interfacing logic through at least a first bus for transmitting at least a first signal from the memory controller to the first interfacing logic, the memory controller being clocked by a second system clock (*fig. 2 items 18, 106, 114-116; column 6, lines 27-57*)" (Office Action at 2); and

(3) "second microprocessor connected to the memory controller through at least a second bus for transmitting at least a second signal from the memory controller to the second processor, the

second bus requiring a first period of time more to transmit the second signal than what the first bus requires to transmit the first signal. . . *(fig 2, items 16, 202, 102, 160, 232-236; column 7, lines 4-60)*" (Office Action at 3).

Applicants respectfully submit that Thaller does not "teach[] the invention substantially as claimed" as the Examiner contends. (Office Action at 2.) In particular, Thaller discloses a "computer system 10 [that] comprises a synchronous system bus 28 which is coupled to first and second CPU modules 14, 16." (Thaller, col. 5, lines 57-58.) Additionally, "each one of the computer system's modules 14, 16, 18, 20, 22, 24, 26 comprises a node on the system bus 28." (Thaller, col. 6, lines 21-23.) Accordingly, Thaller does not disclose a "second microprocessor connected to the memory controller through at least a second bus" as recited in Claim 1.

For at least this reason, Applicants submit that Thaller does not disclose "the invention substantially as claimed." Moreover, the Examiner also admits that "Thaller does not specifically teach the first interfacing logic delaying the first signal by the first period of time so that the first and the second signals are respectively received by the first and the second microprocessors substantially at the same time." (Office Action at 3.) Thus, Claim 1 is clearly and precisely distinguishable over the cited Thaller reference in a patentable sense, and is therefore allowable over this reference and the remaining references of record.

However, the Examiner proposes Burns to supply the elements of the invention missing from Thaller. Burns was cited as assertedly fully disclosing the following: (1) ". . .a system capable of transmitting data to a plurality of processors generating two clock signals, the length of which when traced differ by the amount of tuning etch required to add sufficient delay to the forwarded clock signals transmitted to the processors. . ." (citing *Burns, fig. 4, items 300, 100a-b, 8, 370, 390; column 6, lines 28-67; column 7, lines 1-44*).

The Examiner further stated that it would have been obvious to combine teaches of Thaller and Burns for the purpose of "providing a transmission scheme that offers reliable data transfer between devices while minimizing latency and skew and maximize bandwidth." (Office Action at 3.) Additionally, the Examiner contends that Thaller provides a motivation to combine "by disclosing a bus arbiter that reduces idle time and avoids wastage of bus bandwidth in lines 1-4 of column 5." (Office Action at 3.) Applicants respectfully submit that the Examiner's proposed combination fails to disclose each and every element as recited in Claim 1.

In particular, there is no motivation in Thaller to combine the teachings of Burns and, even if, arguendo, there was motivation to combine, the proposed combination does not disclose each and every element of Claim 1. First, the Examiner's cited motivation in Thaller recites as an advantage of the Thaller invention, "[t]his feature of the [Thaller] invention, allows the processor to complete any ongoing cache access and to gracefully relinquish the cache, without the need for an elongated bus transaction. In this manner, idle time is reduced and wastage of bus bandwidth is avoided." (Thaller, col. 4, lines 66-67; col. 5, lines 1-4). After describing several embodiments of the Thaller invention, Thaller summarizes, "[i]n the above manner, timing and synchronization problems which may result from command errors are avoided, without elongating all bus transactions to the same size as is done in known computer systems. Thus, the computer system 10 of the [Thaller] invention avoids the associated delay and wasted bus bandwidth that results from the elongation of bus transactions." (Thaller, col. 57, lines 63-67; col. 58. lines 1-2.)

Burns, however, recites "a single tuning etch is needed instead of one tuning etch for every communications link. The forwarded clock signal and data are advantageously transmitted via conduction paths in each communications link that are substantially parallel and of equal length." (Burns, col. 3, lines 34-39.) Moreover, "[i]n a preferred embodiment [of Burns], a single tuning

etch advantageously replaces four individual tuning etches that are typically associated with conventional source synchronous clock forwarding schemes." (Burns, col. 3, lines 59-62.) Thus, Thaller "avoids the associated delay and wasted bus bandwidth that results from the elongation of bus transactions," (Thaller, col. 58, lines 1-2), while Burns employs a single clock tuning etch that "advantageously replaces four individual tuning etches." (Burns, col. 3, line 60.)

Accordingly, there is no motivation to combine the teachings of Thaller with the teachings of Burns to approximate the teachings of the present invention. Therefore, as Claim 1 is clearly and precisely distinguishable over the cited Thaller reference in a patentable sense, and there is no motivation to combine Thaller and Burns, Claim 1 is therefore allowable over these references and the remaining references of record. Applicants respectfully request that the rejection of Claim 1 under 35 U.S.C. § 103(a) be withdrawn and that Claim 1 be allowed.

Furthermore, even if there were any motivation to combine the Thaller and Burns teachings, the proposed combination does not teach each and every element as recited in Claim 1. In particular, neither Thaller nor Burns teach "*the first interfacing logic delaying the first signal* by the first period of time so that the first and the second signals are respectively received by the first and the second microprocessors substantially at the same time" with "*a first microprocessor having one or more interfacing logics including a first interfacing logic*" and "a memory controller connected to the first interfacing logic through at least *a first bus for transmitting at least a first signal from the memory controller to the first interfacing logic*," as recited by Claim 1 (emphasis added).

Instead, Burns discloses "*delay in the forwarded clock signal is generated at the transmitting device* by adding tuning etch," (Burns, Abstract, emphasis added) with "the major advantage of [the Burns] technique is that it *eliminates the need to insert tuning etch upstream* to the forwarded clock signal associated with each individual data bundle." (Burns, col. 7, lines 6-8,

emphasis added.) Not only does Burns not disclose the same method or system for delaying a signal as the present invention, Burns teaches generating a delay at the transmitting device. As described above, Claim 1 recites "the first interfacing logic delaying the first signal," where the first microprocessor includes the first interfacing logic and the first bus transmits "at least a first signal from the memory controller to the first interfacing logic." Thus, for at least this reason, the proposed combination of Thaller and Burns does not disclose each and every element of Claim 1. Applicants therefore respectfully request that the rejection of Claim 1 under 35 U.S.C. § 103(a) be withdrawn and that Claim 1 be allowed.

The Examiner employed the same proposed combination and rationale in rejecting Claim 10 under 35 U.S.C. § 103(a). "The same motivation that was utilized in the combination of claim 1, applies equally as well to claim 10. By this rationale claim 10 is rejected." (Office Action at 12.) Applicant respectfully traverses this rejection and submits that the above reasoning that overcomes the Examiner's proposed combination with respect to Claim 1 is equally effective as applied with respect to amended Claim 10. Therefore, as amended Claim 10 is clearly and precisely distinguishable over the cited Thaller reference in a patentable sense, and there is no motivation to combine Thaller and Burns, and the proposed combination does not teach each and every element as recited in amended Claim 10, amended Claim 10 is therefore allowable over these references and the remaining references of record. Applicants respectfully request that the rejection of Claim 10, as amended, under 35 U.S.C. § 103(a) be withdrawn and that amended Claim 10 be allowed.

Claims 2-9 depend on and further limit Claim 1. Hence, for at least the aforementioned reasons, these Claims would be deemed to be in condition for allowance. Applicants respectfully request that the rejections of the dependent Claims 2-9 also be withdrawn. Similarly, Claims 11-18 depend on and further limit amended Claim 10. Hence, for at least the aforementioned reasons,

these Claims would be deemed to be in condition for allowance. Applicants respectfully request that the rejections of the dependent Claims 11-18 also be withdrawn.

New Claims 19 and 20 are allowable for the same reasons as described above. In particular, neither Thaller, Burns, nor the Examiner's proposed combination of Thaller and Burns disclose "a first microprocessor comprising one or more interfacing logics including a first interfacing logic, the first microprocessor being clocked by a first system clock; a memory controller coupled to the first interfacing logic through at least a first high frequency, point-to-point, unidirectional, source-clocked bus for transmitting at least a first signal from the memory controller to the first interfacing logic, the memory controller being clocked by a second system clock; a second microprocessor comprising one or more interfacing logics including a second interfacing logic, the second microprocessor being clocked by a third system clock; the second microprocessor coupled to the memory controller through at least a second high frequency, point-to-point, unidirectional, source-clocked bus for transmitting at least a second signal from the memory controller to the second interfacing logic, the second high frequency, point-to-point, unidirectional, source-clocked bus requiring a first period of time more to transmit the second signal than what the first high frequency, point-to-point, unidirectional, source-clocked bus requires to transmit the first signal; and wherein the first interfacing logic is configured to delay the first signal by a second period of time and the second interfacing logic is configured to delay the second signal by a third period of time so that the first signal and the second signal are respectively received by the first microprocessor and the second microprocessor substantially at the same time" as recited by independent Claim 19.

Accordingly, independent Claim 19 would be deemed in condition for allowance. Claim 20 depends on and further limits Claim 19. Hence, for at least the aforementioned reasons, Claim 20

would be deemed to be in condition for allowance. Applicants therefore respectfully request that Claims 19-20 also be allowed.

Applicants have now made an earnest attempt to place this Application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicants respectfully request full allowance of Claims 1-20.

Applicants do not believe that any fees are due; however, in the event that any fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

Should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

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